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A HYBRID COMPUTING SYSTEM USING THE IBM 1800 DATA ACQUISITION AND CONTROL SYSTEM AND AN ANALOG COMPUTER

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This paper will describe a configuration for a special hybrid system designed for aerospace simulation work. Emphasis will be placed on the utilization of the IBM 1800 Data Acquisition and Control System to control the digital features of a Solid State Analog Computer. These features allow:

1. Direct digital entry and sense of the analog computer's digital patchbay.
2. Direct digital entry and verification of the analog components through the digital logic section.
3. Simplification of the analog patch board.
4. High speed machine readiness checks controlled by the 1800 system.
5. Automation of diagnostic maintenance of the hybrid system.

Programming requirements for a marketable aerospace-oriented hybrid system will be discussed. Capabilities and limitations of the IBM 1800 process controller in a hybrid computing system will be presented with reference to a typical Saturn vehicle simulation task.

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Programming requirements for a marketable aerospace-oriented hybrid system will be discussed. Capabilities and limitations of the IBM 1800 process controller in a hybrid computing system will be presented with reference to a typical Saturn vehicle simulation task.

INTRODUCTION TO THE PROBLEM

The problem is to provide a program supported general purpose hybrid computing system for aerospace simulation work. The following tasks are representative of the areas of application for the system to be described.

- Analysis of vehicle control systems including the simulation of systems
- Study of structure-fluid-thrust coupling in space vehicles
- Lateral loads problems
- Multi-time-point perturbation studies
- Nonlinear six-degree-of-freedom trajectory slides
- Iterative trajectory optimization studies

The advantage of a hybrid system in this application is derived from the combination of the best attributes of digital and analog computation. The digital computer is able to store large amounts of data; to control by way of a stored program the entire sequence of events during computation; and to alter this sequence when appropriate, based upon predetermined criteria. The digital computer has many advantages in generation of functions of two or more variables and in carrying out certain other arithmetic operations. The analog computer has the advantage of high differential equation solving speed, an ease and flexibility in interfacing with external hardware, and a rapport between the engineer and the computer which is difficult to attain with a digital computer.

SOLUTION

After a discussion of the tasks listed in the introduction, the analog computer will be described in sufficient detail to give the reader some insight into the design of the 1800 system. Following the computer descriptions, interfacing and hybrid support programs will be discussed.

A. HYBRID SYSTEM TASKS

This system has been designed for versatility and ease of application to new problem areas as well as to presently encountered problems. The two major components, the analog computer and the digital computer, were each designed specifically for hybrid computation. The combination of the two machines in this system represents a significant advance in the field of hybrid computation. All of the programming features of the analog computer, with the exception of the actual analog signal connections, are controlled by logic level signals which can originate from the input media of the keyboard patchable digital logic signals, the digital computer or paper tape reader. This system makes available, for the first time, a hybrid computer that can truly utilize the high speed parallel analog computational units as subroutines. The flexible digital computer with built-in linkage equipment can exercise complete control over the analog computer--including its patchable digital logic section--for solution of distributed parameter problems, optimization problems, and those requiring perturbation techniques with an ease and efficiency which has heretofore not been possible.

1. Analysis of Vehicle Control Systems Including the Simulation of Systems Utilizing Both Digital and Analog Components

Such problems entail simulation of the dynamics of the vehicle in three to six degrees of freedom, depending upon the objectives of the experiment. Depending upon the complexity of digital control systems being studied, the digital control system can be simulated on either the patchable digital logic or by the appropriate numerical algorithms on the digital computer. In either case, the digital computer can be very effectively used to control the simulation experiments, to set up and check out the problems, to run routine preventive maintenance and diagnostic tests, to perform system readiness tests, to collect data, and to perform analysis of that data. Simulation of analog control systems would normally be done with the analog computer portion of the hybrid system.

2. Study of Structure-Fluid-Thrust Coupling in Space Vehicles

This is an area in which a great deal of work remains to be done in developing efficient simulation techniques. The choice of hybrid computation for this type of problem is a natural one. Such problems, by their very nature, lead to distributed parameter models. The study of flexible structure is accomplished in either one of two ways: modal analysis or finite-difference-differential equation models. The former approach is a numerical technique commonly resorted to when digital computers only are to be utilized; the latter approach is a simulation approach. The simulation of flexible structures with a digital computer alone requires small step sizes

in the independent variable in order to ensure computational stability and any kind of reasonable accuracy; hence, the use of a digital computer alone entails large amounts of computing time. On the other hand, if such problems are solved completely on an analog computer, a tremendous amount of computing equipment is required for accurate simulation of even simple structures. With this hybrid system, the best features of both digital and analog computation can be brought to bear simultaneously on the problem. Furthermore, because of the versatile electronic mode control of the analog computer and the high speed digital-to-analog-conversion capability of the digital computer, it will be possible to perform dynamic simulation studies of such systems, utilizing the analog computer components as computational subroutines under control of the digital computer. This same capability also presents many advantages in the solution of other problems such as heat flow, which are characterized by distributed parameter mathematical models.

3. Lateral Loads Problems

These problems entail the analysis of motion of a flexible vehicle with forces applied both longitudinally and laterally, due to such phenomena as wind shear. Again, as in the previous problem, modal analysis can be resorted to on a limited scale. However, this hybrid system will allow direct simulation of the system, utilizing finite-difference-differential equations for representation of the flexible vehicle. Since this requires two integrations with respect to time, for every mass point used to represent the vehicle, even the largest and fastest general purpose digital computers available today would require

large amounts of time for solution. This hybrid system can obtain comparable accuracies to all digital simulation with great savings in computer time.

It has not been practical in the past to attempt serial-type solutions to such problems, for these solutions require data storage and playback capabilities. This approach also usually requires iterative techniques to satisfy boundary conditions. Although there is much yet to be learned about this subject, several such problems have been successfully solved on the Milgo 4010 computer using this technique, including one in which the lateral forcing function was a moving distributed load. The very high speed capability and precise mode control switching of the Milgo 4010 computer made this approach feasible. The Milgo 4010 analog computer is similar in design to the Milgo 4010 analog computer is similar in design to the Milgo 4100 except the 4010 is a $\pm$ 20v reference computer.

4. Multitime Point Perturbation Studies

This hybrid system will be extremely useful for these studies. This type of problem requires not only high computing speeds, since often many levels of the parameter nominal values are used in the experiment (which requires many runs), but also automatic control of the runs and parameter level selection.

Utilization of perturbation techniques results in a nominal equation, plus a perturbation equation which is often linear. Normally, the characteristic roots of perturbation equations are considerably further from the origin in the s-plane than those of the nominal equation. Consequently,

the perturbation equation normally involves higher frequency terms. The two equations are of the same order and normally the nominal solution is a forcing function in the perturbation equation. It is natural then to allocate the solution of the nominal equation to the digital computer and solution of the perturbation equation simultaneously on the analog computer.

Since one is interested in solutions for several levels of a number of parameters, such studies tend to involve large numbers of runs. From one to the next, the nominal values of the parameters and variables corresponding to the nominal value of the state variables require resetting for the next run. This hybrid system can handle this type of problem very efficiently through the automatic control features provided on the analog computer.

In this same area of interest, it is often worthwhile to derive the separate parameter influence coefficient equations, resulting in a separate equation for each parameter which is to be perturbed. Normally, the solution of the original equation about the nominal parameter values forms a forcing function for the other parameter influence equations. If a large number of parameters is involved, the amount of analog computer equipment required for simultaneous solutions would become excessive. This hybrid system can easily handle this problem by treating the analog computer circuits as subroutines, and through the setup and attenuator setting subroutines, can use the same basic analog circuitry to solve for each of the parameter influence coefficients one at a time or in sets. If the mathematical model is linear in the region of interest, this is particularly simple to do since each of the

parameter influence coefficient equations is of the same form and, therefore, requires the same analog circuitry. Only the servo-set attenuators have to be changed from one run to the next. The method of parameter influence coefficients has received a great deal of attention, but practical work involving this technique has been somewhat limited, due to the large amount of analog computing equipment required (if the solutions are to be produced in parallel) or the large amount of time for setup required (if the solutions are to be produced serially). The hybrid system, because of its function storage and control capabilities, is an ideal tool for this type of study. Such studies yield very important information about the behavior of a solution close to the nominal values of the parameters. It is essential for the design of spacecraft control systems to make these coefficients as small as possible in order to minimize the effect of changes in physical components and the changing environment surrounding the spacecraft during flight.

5. Nonlinear Six-Degree-Of-Freedom Trajectory Studies

A complete six-degree-of-freedom simulation requires a large amount of analog computer equipment if performed on an all-analog basis, and the obtainable accuracies leave much to be desired. This is the type of problem that gave rise to the earliest hybrid computer designs. The particular features of this hybrid system, which the engineer will find of particular interest for this application, are:

a. Six of the analog integrators are specifically designed for simulation of systems with natural frequency ranges of 0.001

radians per second in order to allow use of the analog computer for solution of the translational equations of motion if desired.

b. Precise interval control of sampling, via a digitally preset interval timer.

c. A Time-Sharing Executive System which allows off-line jobs to be handled by the digital computer when time is available from the on-line simulation task.

It has been found that the major sources of error in the solution of orbital and trajectory equations with the modern day analog computer arise from errors in attenuator settings, capacitor leakage resistance, capacitor dielectric absorption, and finite gain of the operational amplifier.

Several ways have been found to compensate for these analog computer errors at the very low frequencies. Those having to do with design of the integrators have been incorporated into six specially designed integrators in this hybrid system, thus allowing the use of the analog computer for integration of the translational equations as well as the rotational equations if desired.

6. Iterative Trajectory Optimization Studies

This type of problem requires a high speed analog computer, precise and repeatable computation of the nominal trajectory, and high speed control of the analog computer. Some of the particular features of this hybrid system are:

a. The Milgo 4100 is an extremely high speed computer, maintaining accuracy and full scale output ability to 1000 cps.

b. The IBM 1800 computer is ideally suited for generation of the nominal trajectory; its built-in linkage system provides for precise control of the analog computer, as well as high speed exchange of data.

B. ANALOG COMPUTER

The analog computer selected for this system is the Milgo 4100. The 4100 is a solid-state, ±100-volt reference machine. All operations are accomplished within an accuracy tolerance of 0.01 per cent, and the phase shift of any operation is less than 0.05° at 1 Kc. The analog and digital patch panels being supplied for the IBM, Huntsville Simulation Laboratory allow the full expansion capability specified below in Table 1.

TABLE 1. ANALOG COMPUTER FULL EXPANSION CAPABILITY

Equipment	Quantity
Analog Components:	
Integrating/Summing/Special Purpose Amplifiers	40
Integrating/Summing Amplifiers	20
Summing/High Gain Amplifiers	60
Dual-Input Summing Amplifiers	20
Extended Range Servo-Set Attenuators	30
Standard Servo-Set Attenuators	290
Manual Attenuators	40
Electronic Multipliers	40

TABLE 1--Analog Computer Full Expansion Capability (Continued)

Equipment	Quantity
Function Generators	40
Electronic Resolvers	8
Hard Limiters	16

All nonlinear components, such as multipliers, resolvers, and function generators, are in a Class "O" configuration; that is, all necessary operational amplifiers are included.

Equipment	Full Expansion
Digital Components	
NOR/NAND Elements	100
Monostable Multivibrators	8
Master Counter (6 BCD digits)	1
Fixed Clock	1
Variable Clock	1
Digital Function Switches	20
Access Logic Latches	40
Indicators	20
Trunks	
Addressable Analog Trunks	140
Hardware Trunks	28
Digital Trunks	40
Analog-to-Digital Patch Bay Trunks	20

Equipment	Full Expansion
Control Equipment	
Analog Computer Command Entry Subsystem	1
Digital Voltmeter and Readout	1
Analog Function Switches	20
Oscilloscope, Tektronix	1
Paper Tape Reader	1
Paper Tape Punch	1
Transistorized Voltmeter	1
Peripheral Equipment	
Brush eight channel recorders	4
X-Y Plotter	4
Display Scope	1
Printer	1

Extensive capability for external digital control and monitoring makes the Milgo 4100 attractive for use in a hybrid configuration. Control and information transfer are possible between the digital computer and three different areas of the analog computer: (1) Analog Computer Command Entry Programming Technique, (2) the digital patchbay, and (3) the analog patchbay.

1. Analog Computer Command Entry Programming Technique (ACCEPT)

In addition to providing the means for external control of servo set attenuators, scan of pertinent analog signals and mode selection, the

ACCEPT provides an additional feature which is unique in its extent in analog computers available today. This feature is function control. The function of multipurpose (combination) amplifiers, multipliers, resolvers, and the stage of a group of logic control terminals are programmable through the ACCEPT I/O channels. The various functions and states under digital control follow:

TABLE 2. ANALOG UNITS AND PROGRAMMABLE STATES

Analog Unit	Programmable States			
Combination Amplifier	Integrator	Summer	Special Purpose Integrator (mode & scale) selection via patchable logic)	
Summing Amplifier	Summer	High-Gain Amplifier		
Multiplier	Multiplier	Divider	Square Unit (two squares)	Square Root Unit
Resolver	Polar-to-Cartesian Conversion (2 multipliers released)	Cartesian-to-Polar Conversion	Sine-Cosine Generator (4 multipliers) released)	Cartesian Axis Rotation
Logic	"0" State	"1" State		

The assigned state of each computer unit is continuously displayed on a rear-lit status panel in the central console area. A combination amplifier, for example, will appear as "INT," "SUM," or "SP" depending upon the most recent instructions from the keyboard, digital computer, or paper tape reader.

Each component will remain in the most recently determined state until commanded to a different one via any of the means of entry. Switching to the various functional states is accomplished with bistable, mercury-wetted relays which provide a memory and protect against any loss of programmed status due to shutdown or inadvertent loss of computer power.

All command entries to ACCEPT, from any source, may be recorded in permanent form by a printer and may be simultaneously punched on paper tape for use in reinserting the problem on another occasion. In addition, when receiving data from the digital computer, a verification in the form of a return address is supplied to the digital computer to verify that the original command actually accomplished the desired result.

The message formats for word transfers in and out of ACCEPT are shown in Fig. 1.

2. Digital Patchbay

The digital patchbay makes available the input and output connections for all the patchable digital logic. This logic consists of 100 NOR/NAND logic blocks, a six-decimal-digit BCD counter, a variable frequency clock, and eight monostable multivibrators. Two adjacent NOR/NAND logic blocks may be connected together using two bottle plugs to form a bistable circuit. This panel also terminates the time scale and mode control inputs for integrators in the special purpose state. Control signals may be sent to the input/output equipment via this patch panel; for example, recorder start-stop, recorder speed, paper tape reader start-stop, paper tape punch

perforate, and the oscilloscope trigger. Logic level outputs of the analog comparators are also brought out on this panel.

Using patch panel programming, the digital logic initial states, special purpose integrator time scales, and modes and input/output devices may be controlled from 30 latches set or reset in ten-bit bytes through the ACCEPT channel or directly from the #1 data channel of the 1800 computer.

3. Analog Patchbay

All analog computing elements are terminated at the analog panel. Also located here are inputs to all the analog output devices as well as external trunks and a trunk to the digital panel.

The use of digital hardware to select and store analog computing element functions and the inclusion of operational amplifiers in the resolvers, multipliers, and diode function generators eliminates a significant amount of extraneous patching on the analog problem boards.

The hole area is only ten per cent of the total panel area. Holes are located on 0.390 inch centers and hole diameters are 0.144 inch. Ample room is thus afforded for adequate lettering of computer element functions between holes and all lettering can be read even in a fully patched area.

This design approach makes the patched problem math flow more apparent to the operator-analyst.

4. Additional Milgo 4100 Features

Two other capabilities of the Milgo 4100 are, at this time, unique analog computer features.

a. System Scaling Indicator (SSI)

A feature of the overload indication system, SSI is a means of providing the operator with an indication of marginal scaling. This system allows the operator to check for amplifiers operating above five selectable divisions of reference. These divisions are set at 0.25, 0.50, 0.75, 1.0, and 1.1 times reference. Activation of this checking system at any of these five levels does not affect the dynamic amplitude operating range of the amplifiers.

An example of how this system is used follows:

When a problem which has just been patched is to be scaled effectively for test inputs, two operating criteria are set:

(1) No amplifier output shall exceed 75 volts (for example) under test values.

(2) No amplifier output shall be less than 25 volts (for example) at its peak value for test values.

With these two criteria in mind, SSI is used by depressing the 75-volt button, allowing the problem to run for a sufficient period of time, and inspecting the amplifier overload indicators to determine which amplifier outputs have exceeded 75 volts during this test run. Those amplifiers are rescaled and the procedure repeated until no amplifier output exceeds 75 volts.

The second criterion is evaluated by depressing the 25-volt pushbutton, running the problem again for the test period, and inspecting the overload panel for amplifier outputs which did not exceed 25 volts. Any amplifier output which did not exceed 25 volts during this run should be rescaled for better use of the computer dynamic range. Once this rescaling is accomplished, another check at 75 volts should be made to assure that amplifier outputs still do not exceed 75 volts during the test.

This test accomplished, the problem is ready to run with the knowledge that no amplifier outputs are "in-the-mud" and that every amplifier output has sufficient dynamic range allowed for unusual reactions to parameter perturbations.

b. Extended Range Servo-Set Attenuators

This attenuator is a unique device allowing scale factor settings to five significant digits while still maintaining the 0.01 per cent accuracy desired. This attenuator allows settings from zero through 9.9999, still maintaining the 0.01 per cent signal accuracy. (With standard attenuators, accuracy is lost when an operator desires a setting greater than unity; for example, 4.2517. In such cases, the method would be to connect the attenuator wiper, set to 0.4252, to a gain of ten input of an amplifier. Since the attenuator output error is amplified by a factor of ten, a setting error of 0.01 per cent becomes a 0.1 per cent error at the output of the amplifier.)

The output of an extended range attenuator is connected directly to the summing junction of an amplifier. Highly accurate resistors, switched under digital control, are provided for the units digit of the setting. The servo-driven helical potentiometer represents only the fraction. This system permits five-digit accuracy.

C. DIGITAL SECTION OF THE HYBRID SYSTEM

The 1800 Data Acquisition and Control System represents one of IBM's most advanced problem solving systems, geared to record and measure data as it occurs. Featuring SLT circuitry, this system provides great speed, reliability, and economy. The modularity of the 1800 allows the system to be designed for peak performance in the initial configuration which can be readily modified for growth and desired changes. The wide variety of input/output units, standard to the 1800 system, makes the 1800 an ideal choice for use in a hybrid computing system. The Processor Controller, in this system, combines a 2-microsecond, 8 K memory (expandable to 32 K) with 5 fully buffered highspeed cycle stealing input/output channels (expandable to 9 channels). This provides capability for asynchronous I/O operation at up to 500,000 words per second. Other features of the 1802 Processor Controller include three index registers; indirect addressing; up to 384 interrupt channels arranged in up to 24 priority levels; and three interval timers that can be started/stopped and preset to any value to asynchronously control timed event sequences. The word format of 16 bits plus a parity bit and a storage protection bit, together with the capability for arithmetic operation with 32-bit

double length and 48-bit extended length, is optimum for hybrid system usage. A 16-bit format allows address and data transfer between the digital and analog portion of the system to be carried out with a minimum of wasted bits. The storage protection bit provides the user with the ability, for the first time, for word-by-word protection under program control for data stored in the digital computer memory. The hybrid system user is thus freed from the troublesome possibility of losing valuable data stored in the memory. The available choices of 16-bit single precision, 32-bit double length, and 48-bit extended length arithmetic operation enable the programmer to tailor a program to a wide variety of accuracy requirements. Assembly, utility, and subroutine programs complement the equipment capabilities of this system.

1. The IBM 1800 Process Controller

The IBM 1800 in this hybrid system has 16 K of core storage and a memory cycle time of 2 microseconds. The standard hardware operations are performed in either 16-bit or 32-bit double length words. The minimum add and subtract time is 4.5 microseconds. Multiply time is 14.25 microseconds and divide time is 42.25 microseconds. Program floating point and double precision multiply/divide are standard features. This feature provides a multiply product of 48 bits and a division quotient of 32 bits. Three interval timers are standard on the 1800. These timers may be started, reset, or stopped by the program. A program interrupt can occur when any timer steps down to zero. The basic increments, which can be different for each

timer, are 0.125, 0.25, 0.5, 1, 2, 4, 8, and 16 milliseconds. The increment for each timer can be specified by the customer. The WAIT instruction can be executed to put the computer in an idle condition without affecting the timers and interrupt capabilities. The 1800 word consists of 18 bits. Sixteen bits are used for instructions and data flow purposes. One bit is used for Odd parity and covers both the 16 bits of data and the memory protect bit.

One bit of every word in core storage is used for memory protect. When the memory protect bit is set to "one," a "read only" condition exists. This is a standard feature which is under control of the Write Storage Protect Switch on the console and the program. The memory protect feature greatly enhances the 1800 for hybrid computation. If the program attempts to write in a "read only" protected location, a high order interrupt will occur. If a Data Channel attempts to write in a protected area, a protection violation indicator will be set in the Channel Status Word and cause an interrupt. In both cases, the data in the protected location is not changed.

2. Instruction Word and Addressing

The 1800 system provides two basic instruction word formats. One-word and two-word instructions can be used in the programming of the 1800.

The core storage addressing features the wraparound of memory locations. This means that the next sequential address above the highest numbered address in core storage is always 00000.

Indirect addressing and automatic address modification are standard features on the IBM 1800.

The recognition of an instruction for indirect addressing is accomplished with one control bit in a two-word instruction. When this bit is set to "one," the address portion of an instruction will be treated as an indirect address. Address modification is accomplished with three index registers which are standard features. Two index tag bits in the instruction word are used to address the proper index register. The two index tag bits appear in both the single- and double-word instruction format.

3. Input/Output (I/O) Control

The IBM 1800 system provides two fundamental methods for communication with I/O devices. The first means of I/O control is through a fully buffered hardware data channel. Three data channels (DC's) are standard with expansion capabilities to nine channels.

The DC operates in a cycle-steal mode to give a maximum data rate of 500,000 words per second. The cycle-steal mode of operation provides a powerful means of I/O communications with core storage. Whenever the DC requires storage access, the processor operation is suspended for one memory cycle time. During this time (2 microseconds), one 16-bit word is transferred to or from the specified address in memory. Access by the DC can occur at the end of any memory cycle, and does not change the logical state of the processor. When the DC is satisfied, normally after one memory cycle, the stored program execution proceeds.

An Execute I/O instruction will load the address register and word counter in the channel selected. This will initiate the asynchronous

operation in the cycle-steal mode to transfer data to or from memory via a 16-bit channel data register and the I/O device. The data transfer will continue until the word counter reaches zero. At this time the channel will be either de-selected or data chaining can occur. Data chaining permits the channel to address other blocks of data in memory and to continue data flow. Only two memory cycles (4 sec) are required to execute data chaining. This is called the scan control mode of operation.

The DC scan operation is controlled by two modifier bits in the word stored in the DC word count register. Also, this word can initiate an interrupt at the end of each scan of data.

In order to provide the most versatile hybrid computing system this system includes the use of five 1800 high-speed data channels. These data channels, in conjunction with the conversion equipment, will provide an integrated link between the analog and digital computers to give precision control of all data transfer. Via data channels, the 1800 will have direct communication with the ACCEPT area of the analog computer, the digital patchbay, and the analog patchbay (Fig. 2)

The following hybrid functions are efficiently accommodated

- Set attenuators.
- Readout any selectable terminal of the analog patchbay.
- Make calculations between problem runs, adjust problem runs, and adjust problem parameters as a result of calculation.

- Provide sense and control.
- Provide programmed mode control.
- Provide control over sampling rate of conversion and linkage equipment.
- Perform static and dynamic tests on the entire system.
- Change the assigned state of analog computing elements.

The 1800 system provides for twelve interrupt levels as a standard feature. Sixteen interrupt sense lines can be attached to each interrupt level. In this system, sixteen sense lines are provided in four levels of interrupt.

The interrupt philosophy of the 1800 system is to group interrupts of the same relative priority in the same level. This reduces the number of branch routines required to service the interrupt conditions. This feature allows all interrupt requests common to the specific level to be interrogated and serviced before the Branch Out operation occurs. The same interrupt subroutine can be used for all interrupts on the same level.

The first request on any interrupt level is serviced before another interrupt on the same level or lower will be serviced.

Interrupts on a higher priority interrupt level will temporarily terminate the servicing of a lower level interrupt. Service is returned to the initial request only after all higher order level requests have been serviced.

4. Conversion and Linkage Equipment

The IBM 1800 conversion and linkage equipment configured for this hybrid computing system provides 16 analog-to-digital conversion (ADC)

channels and 16 digital-to-analog conversion (DAC) channels.

The 16 ADC channels are multiplexed with a solid state multiplexer and include sample and hold at the operator's option.

The 16 DAC channels are register buffered to permit simultaneous updating of the 16 channels.

Provision is furnished for expansion to 32 ADC and 32 DAC channels with no additional enclosures required.

a. Digital-to-Analog Conversion

The format for digital-to-analog conversion is 13 bits plus sign with a conversion time of 20 microseconds. The 16 digital-to-analog converters are supplied with data by a data channel. Use of a data channel minimizes degradation of the processor-controller performance by allowing data transfers from memory on a cycle-stealing basis. Also, the program is released from the word count and memory address updating workload.

b. Analog-to-Digital Conversion

The analog-to-digital conversion equipment will accept inputs of $\pm$100 volts and have an error not exceeding 0.06% $\pm$ 1/2 LSB. Program selectable resolutions of 8, 11, and 14 bits are standard features of the 1800 system. ADC conversion times are as follows, dependent upon the program selectable resolution.

8 bits + sign, 29 microseconds

11 bits + sign, 36 microseconds

14 bits + sign, 44 microseconds

c. Linkage Timing

The system is provided with a periodic sample mode. The period of time between samples in the ADC link, and the delay from sample time until the DAC's are updated, are accurately controlled by digital timing equipment located in the 4100 computer. Time periods controlled by this timing equipment are variable under manual control or under digital computer program control through the 4100 ACCEPT system.

Through the use of the discretes, interrupts, and digital patchable logic, the sample-to-sample and the sample-to-update intervals are also controllable from the digital computer.

All analog channels to the analog computer are capable of being updated simultaneously.

Sample and hold amplifiers provided for interface use between the analog computer and the ADC input to the digital computer are terminated in the form of a single input and a single output connection on the analog patch panel of the Milgo 4100.

The output termination is located adjacent to its corresponding ADC input channel in order that it may be easily connected. Logic control for the sample and hold amplifiers is terminated on the logic patch panel and may be connected to operate in accordance with computer command or master clock command.

Full digital buffering for each DAC is provided to allow simultaneous updating of the 16 DAC outputs. Non-return-to-zero transfer from the buffers to the DAC registers is utilized to minimize switching transients.

5. Special Features and Options

The modular construction of the 1800 system permits orderly expansion. Therefore, as the requirements change for the hybrid system, additional equipment can be added with minimum interference to operating time.

The system has certain inherent expansion capabilities in the conversion equipment which will permit expansion without additional enclosures.

The optional expansion of the ADC points to 32 can be accomplished by installing one additional 16-point multiplexer with control in an existing enclosure.

The optional expansion of the DAC points to 32 can be accomplished by installing 8 two-point digital-to-analog converters with control in an existing enclosure.

The 16 interrupt points can be expanded to 48 points with 12 levels of interrupts. This is accomplished by adding 32 interrupt points, with their associated controls to the system.

The 1800 equipment required for this hybrid system is listed in the appendix.

D. INTERFACING

1. Digital Data

Digital data can be transferred from the analog computer to the IBM

1826 Data Adapter with no special adapter hardware on the data lines. This is due to the wide range of input levels acceptable at the digital input (voltage option) points. However, digital outputs pose a minor problem. The 0, +3v levels will be converted in the analog computer to -12, 0v levels. All adapting of control line timing and electrical driver/receiver characteristics will be accomplished by the analog computer manufacturer to meet IBM interface specifications.

2. Analog Data

Sample and hold amplifiers for the inputs to the high level multiplexer are not a standard feature of the 1826. Therefore, the sample and hold capability is included in the analog computer. From an operational viewpoint this is a reasonable location for sample and hold elements, as these units are often used by analysts operating an analog computer in a stand-alone mode.

High speed, high level analog inputs to the IBM 1826 Data Adapter are available only in single ended form. Isolation of the Milgo 4100 signal ground from the IBM 1826 signal ground has been accomplished by including a special set of 16 differential amplifiers in the sample and hold package located in the analog computer.

E. HYBRID SUPPORT PROGRAMS

The program support required for a marketable hybrid simulation system includes many of the announced 1800 support programs. The purpose of this section is to identify the available 1800 programs which are of particular interest to the hybrid user and suggest additional routines required to complete a hybrid program package.

Personnel using a hybrid system are usually engineers who must work closely with the simulated system on the computers, both to assess the validity of the result and to obtain insight into the nature of the problems involved with the physical system. Hybrid computation, by its very nature, precludes the method of operation often used for digital scientific computing centers of having the engineer describe the problem to a team of programmers who in turn put the problem on the computer. Therefore, one of the basic requirements for a successful hybrid computing center is the availability of easy-to-use systems programs, compilers, assemblers, library and utility routines, and standard operational routines that can be called by the engineer-programmer in either symbolic or problem oriented language programs. Perhaps the most difficult task encountered by the hybrid system engineer is the proper allocation of tasks between the analog and digital computers for a particular study. Characteristic root analysis has been found to be the most efficient approach to this problem. This entails linearization of the given model by suitable approximations and application of perturbation techniques. A root finder program, which locates the poles and zeros in the plane for linear transfer functions, is furnished as part of the IBM 1800 subroutine library. This includes the transformal mapping of pole-zero locations in the z-plane to facilitate the study of sampled data systems and/or systems that utilize digital controllers.

1. Announced Programs

a. IBM 1800 Assembler Language

The IBM 1800 Assembler Language provides the programmer a

flexible and meaningful symbolic language that is easier to code than a binary machine language. This is a two-pass assembler which incorporates a compressor program to compress symbolically assembled output into a form suitable for execution. It provides for assembly of both absolute and relocatable mainline programs and for assembly of relocatable subroutines. By means of ENT and CALL statements, provision is made for automatic symbolic cross-referencing between programs at load time. The assembler may be used to generate subroutines and subprograms for Fortran programs and may call Fortran subroutines as well as subroutine library and utility routines.

b. IBM 1800 Fortran Language

The Fortran compiler furnished with the IBM 1800 Computer accepts programs written in the Fortran IV language. It is a subset of the Fortran IV language used with the 7000 series of IBM computers. It does not provide for double precision or complex variables, but, except for these minor restrictions, is the same as the standard Fortran IV language.

c. IBM 1800-2310 Nonprocess Monitor System

The 1800-2310 Nonprocess Monitor System, a disc-oriented system, allows the user to assemble, compile, and/or execute individual or several programs with a minimum of operator intervention. Jobs to be performed are stacked and separated by control records

that identify the jobs. The monitor system also provides the flexibility to program for the diverse applications of real time simulation and data acquisition. The 1800-2310 Nonprocess Monitor System is composed of five separate programs: supervisor, subroutine library, disc utility, assembler, and Fortran compiler. This programming system requires the 2310 Disc Storage Drive.

d. IBM 1800 Subroutine Library

The 1800 subroutine library provides arithmetic, functional, code conversion, I/O control, and selective dump subroutines for use by object programs generated by the 1800 assembler or the 1800 Fortran compiler.

The floating point subroutines in the subroutine library offer two ranges of precision: 23 bits or 31 bits of precision. Included are floating point-fixed point conversion, code conversion, I/O control, selective dump, and any number of special functions. (See Form C-26-5880-2, entitled "IBM 1800 Subroutine Library" for a complete description of the subroutine library.) It is important to note that, as part of the standard library subroutines, analog input and output routines are provided. There is also a special set of Fortran-oriented subroutines which is used as linkage between a Fortran CALL statement and certain of the analog/digital subroutines. These linkage subroutines allow the engineer-programmer to gain access to the analog/digital input/output subroutines through simple CALL statements.

e. IBM 1800 Utility Routines

The 1800 Systems Utility Routines are part of the basic programming system to be used by all IBM 1800 installations. These programs make it possible to program the 1800 for a wide range of data acquisition and real time control and simulation applications. The utility routines include an I/O routine for normal I/O of digital information, dump routines, and loader routines, including a relocating loader, a core image converter, and a core image loader. These routines provide the programmer with a versatile tool for transferring data from one medium to another and for performing the repetitive utility functions needed daily for most data processing installations. They also include routines to aid the user in debugging his programs.

f. IBM 1800 Time Sharing Executive System

The Time Sharing Executive System is a real time process control and hybrid simulation programming system that affords the user an easy means of generating, testing, and executing complete real time programs.

With this system the user can write simulation programs in Fortran language or the 1800 assembler language. The Executive System provides for simulation of external interrupts and analog input/output to enable testing of programs without exercising the rest of the hybrid system. It also provides for designation of memory protected programs in core or on disc.

The Time Sharing Executive Routine operates with the hybrid simulation control program in complete control at all times. When time is available in the simulation program, that time may be used for execution of nonsimulation programs operating as a monitor system.

2. Hybrid Operating System

The entire package will be designed to run under control of a single Hybrid Executive monitor which provides the option of calling subprograms under keyboard or CALL-card control. The basic subprograms required are as follows:

- Static and Dynamic Analog Computer Diagnostics
- Static Linkage Diagnostics
- Card Set DGF Setup Program
- Hybrid Compiler and Utilities

a. Static and Dynamic Analog Computer Diagnostics

This program or group of programs will test the significant characteristics of every computing element. The program should have sense switch options for:

(1) Stop on detected failure.

(2) Print error condition in clear text called from disc or tape.

(3) Looping test on failing element to aid troubleshooting.

The technique used for these tests involves patching three amplifiers, one electronic switch, one comparator, and a small number of diodes and attenuators together to form a multipurpose

"probe." This "probe" is capable of sensing offset, gain, and noise, and of developing a discrete logic signal if the measured input is out of tolerance. The address of any computing element found to be out of tolerance is printed out. The 1800 controls the functional state of analog components, inputs to the analog computer components under test, a limited number of changes to the patched configurations by the use of electronic switches, and connection of the "probe" to points under test.

The following tables contain the static and dynamic readiness checks that will be performed to assure analog system readiness each morning.

TABLE 3a. STATIC AND DYNAMIC READINESS CHECKS

Analog Computing Element		Checks Performed
Summing Amplifiers		Offset, gain, noise, and ability to switch to high gain function
Combination Amplifiers	Summing status	Offset, gain, noise
	Integrator status	Dynamic integrator test for all time scales
	Special purpose integrators	Dynamic integrator test for all time scales controlled from digital patch bay
Attenuators		Settability at three points
Multipliers	Multiply	Accuracy for nine sets of input values
	Divide	Accuracy for eight sets of input values
	Square	Accuracy for two input values
Limiters		Check output of limited amplifier with ±1.0 reference inputs, and limits set to ±0.5 reference
Extended Range Attenuators Extended Range Attenuators		One of the extended range attenuators is set to 0, 0.5, 1.5, 2.5, 3.5, 4.5, 5.5, 6.5, 7.5, 8.5, and 9.5 to test the extended range decoding subsystems. All others will be checked at 0 and 9.5.

TABLE 3b

STATIC AND DYNAMIC READINESS CHECKS

Analog Computing Element		Checks Performed
Resolvers	Cartesian to polar	Conversion accuracy is checked at the following (x, y) points: (+0.2, +0.2), (+0.2, -0.2), (-0.2, -0.2), (-0.2, +0.2), (0, 0), (1, 0) and (0, 1)
	Polar to cartesian conversion status	Conversion is checked at the following (R, θ) points: (1, +0.25), (1, +0.75), (1, -0.25), (1, -0.75), (0, +0.25), (1, 0) and (0, 0).
	Sin-Cos function generation status	Function generation accuracy is checked at θ=0, ±0.25 and ±0.75.
	Rotated form	Rotation is checked at the following (x, y, θ) points: (+0.2, +0.2, +0.25), (+0.2, +0.2, +0.75), (+0.2, +0.2 = 0.25), (+0.2, +0.2, -0.75) and (+0.2, +0.2, 0).

b. Linkage Diagnostics

This program provides maintenance personnel with the I/O characteristics of the digital to analog, analog to digital, and discrete linkage equipment.

c. Hybrid User Utilities

The hybrid programmer must have at his disposal an extension of the normal compiler language statements to allow him to set up and communicate with the analog computer portion of the system. This augmented set of statements will operate within an executive monitor system which provides for on-line corrections in the compiler language from keyboard or cards.

The hybrid programmer is, with a minimum keyboard CALL-card entry, able to store the analog computer setup on disc, tape, or cards. Recall of this setup is also made as easy as possible.

An example of a typical set of hybrid statements is shown in the following tables.

TABLE 4

HYBRID OPERATING SYSTEM

Section I

LEVEL I SUBROUTINES

(Machine independent, user oriented, written in Truncated Fortran)

SUBROUTINE	LINKAGE	SUBROUTINES CALLED	FUNCTION
POTS (I, X)	I = Address X = Value	FTOM, OUT	Sets potentiometer No. I to value X.
POT (I, X)	I = Address X = Value	OUT, IN, MTOF	Reads Potentiometer No. I. X is set equal to voltage at wiper of attenuator.
AMPS (I, N)	I = Address N = Logic State	OUT	Sets amplifier No. I to Logic state N, where, N = 0, Integrate N = 1, Sum N = 2, High gain N = 3, Special purpose
AMPL (I, N)	I = Address N = Logic State	OUT, IN	N is set equal to logic state of amplifier I. N corresponds to code of AMPS.
AMPA (I, X)	I = Address X = Value	OUT, IN, MTOF	X is set equal to the voltage output of amplifier No. I.
AMPIR (I, X)	I = Add X = Value	OUT, IN, MTOF	X is set equal to the initial rate of integrator No. I.
MULTS (I, N)	I = Add N = Logic state	OUT	Set multiplier I to logic state N, where N = 0, multiplication N = 1, division N = 2, square N = 3, square root

SUBROUTINE	LINKAGE	SUBROUTINES CALLED	FUNCTION
MLTL (I, N)	I = Add N = Logic state	OUT, IN	N is set equal to logic state of multiplier I. N corresponds to code of MULTS.
MULTA (I, X)	I = Add X = Value	OUT, IN, MTOF	X is set equal to voltage output of multiplier No. I.
RESOL (I, N)	I = Add N = Function state	OUT	Sets resolver I to function N, where N = 0, polar to cartesian N = 1, cartesian to polar N = 2, sine-cosine N = 3, rotated coordinates
RESL (I, N)	I = Add N = Function	OUT, IN	N is set equal to function state of resolver I. N corresponds to code of RESOL.
RESI (I, X)	I = Add X = Value	OUT, IN, MTOF	X is set equal to voltage of resolver I. Note: I is of the form NNM where NNO is the resolver address and M is the terminal number where M = 1, 0 if in C-P mode M = 2, R if in C-P mode M = 3, R cos 0 if in P-C mode M = 4, R sin 0 if in P-C mode M = 5, cos 0 if in S-C mode M = 6, sin 0 if in S-C mode M = 7, μ if in ROT mode M = 8, V if in ROT mode
LIMIT (I, TL, BL)	I = Add TL= upper lim BL = lower lim	FTOM, OUT	Sets upper and lower limits on limiter I, where I is address of upper pot. A check is made to ensure validity of limiter address.

HYBRID OPERATING SYSTEM

Section I (continued)

SUBROUTINE	LINKAGE	SUBROUTINES CALLED	FUNCTION
LOGIC (I, N)	I = Add N = 1, True 0, False	OUT	Set logic state of I equal to N.
STATE (I, N)	I = Add N = Array of 10 logic states where; 1 → True 0 → False	OUT, IN	Array N is set equal to the logic state of each element on the I level. Suppose I = 320, then N(1) = L.S. of elem. 320 N(2) = L.S. of elem. 321 . . . N(10) = L.S. of elem. 329
RESET		OUT	Puts computer in reset mode.
HOLD		OUT	Puts computer in hold mode.
OPER		OUT	Puts computer in operate mode.

TABLE 5

HYBRID OPERATING SYSTEM

Section II

LEVEL II SUBROUTINES

(Machine Independent, Intermediate, Truncated Fortran)

SUBROUTINE	LINKAGE	SUBROUTINES CALLED	FUNCTION
FTOM (X, M)	X = Floating pt. value M = Array of 6 elements		Takes X and converts to fixed point (X may contain 4 decimal places and one integer). Then M(1) = 1, if X is neg.; M(1) = 0, if X is pos. Elements 2 → 6 of M then contain one digit each of X.
MTOF (M, X)	X = Flt. pt. value		Converts M to floating X. M is defined as in FTOM.

TABLE 6

HYBRID OPERATING SYSTEM

Section III

LEVEL III SUBROUTINES

(Machine oriented, coded in machine language)

SUBROUTINES	LINKAGE	FUNCTION
OUT, (KONT, IT, IND,	KONT = Control number which sets first 4 bits of first access word	Builds one to three 16-bit ACCEPT words and inputs them to Milgo 4100 Analog Computer. (Uses Boolean logic.)
	IT = Analog group element number (ATT, AMP, etc.)	
	IND = -1, status set -2, magnitude set 0, logic read and mode set +, status or magn. read	
	IA = Address of element	
	MORS = Magnitude or status depending on IND	
IN (IND, MORS)	IND = -1, status read 0, magnitude read +1, logic read	Reads in two or three ACCEPT words from Milgo 4100, deciphers these words, and sends back MORS.
	MORS = An array whose length depends on IND.	
	IND = -1, array 1 long 0, array 6 long +1, array 10 long	

SUMMARY

The IBM 1800 and Milgo 4100 hybrid system combines two machines which were developed with hybrid applications as important criteria. The salient features and limitations follow:

IBM 1800 Data Acquisition and Control System

The linkage equipment is a part of the 1800 system, which means that the linkage will be fully documented, as are the process controller and analog computer. Standardization of the linkage hardware has reduced the need for special hardware and programming. Linkage equipment in the field has historically remained in the development phase through most of the useful life of a hybrid system. The modularity in design of the IBM linkage provides a capability for rapid and reliable systems expansion.

The word-by-word memory protection feature and the low cost disk file capability of the IBM 1800 are usually attractive features to the hybrid user.

Configuring a hybrid system with the 1800 is complicated to an extent by the lack of a $\pm$100-volt hybrid analog output feature, and the lack of a $\pm$100-volt hybrid differential input feature on the 1800 linkage.

This problem was resolved by providing the necessary equipment in the analog computer.

Milgo 4100 Analog Computer Consists of the Following Equipment

(1) System Scaling Indicator

This equipment provides an effective method for the detection of marginal scaling.

(2) Extended range servo set attenuators

(3) ACCEPT

This digital input-output section of the 4100 allows extensive digital control and sensing of the analog computer by the IBM 1800

The two computers linked together in a hybrid mode, plus the mentioned application and programming support, combine to make one of the most versatile hybrid computing systems in the 1800 price-performance class.

ACCESS WORD CODE

INPUT TO ACCESS

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	1ST WORD	ADDRESS (1) MODE CONTROL (0)	PROGRAM (1) READ (0)	ANALOG (1) LOGIC (0)	E(8)	E(4) RESET	E(2) HOLD	E(1) OPER	A(800)	A(400)	A(200)	A(100)	A(10)	A(40)	A(20)	A(10)
B	X			SIGN - (1) + (0)	A(8)	A(4)	A(2)	A(1)	M(2)	M(4) S (4)	M(2) S (2)	M(1) S (1)	M(.8)	M(.4)	M(.2)	M(.1)
C	X				M(.08)	M(.04)	M(.02)	M(.01)	M(.009)	M(.004)	M(.002)	M(.001)	M(.0008)	M(.0004)	M(.0002)	M(.0001)
D	1ST WORD	ADC (1) LOGIC			E(8)	E(4)	E(2)	E(1)	A(800)	A(400)	A(200)	A(100)	A(80)	A(40)	A(20)	A(10)
E	X			SIGN -(1) +(0)	A(8) L.XX8	A(4) L.XX4	A(2) L.XX2	A(1) L.XX1	M(8) L.XX8	M(4) L.XX4	M(2) L.XX2	M(1) L.XX1	M(.8) L.XX8	M(.4) L.XX4	M(.2)	M(.1)
F	X				M(.08)	M(.04)	M(.02)	M(.01)	M(.008)	M(.004)	M(.002)	M(.001)	M(.0008)	M(.0004)	M(.0002)	M(.0001)

OUTPUT FROM ACCESS

LEGEND

E = Analog Element Number (ATT, AMP, ETC)
A = Address Number
M = Magnitude
S = Analog Element Status
L = Logic Readout (XX = First Two Digits Called Out in "A" Of First Word)

FIGURE 1. ACCEPT WORD FORMATS

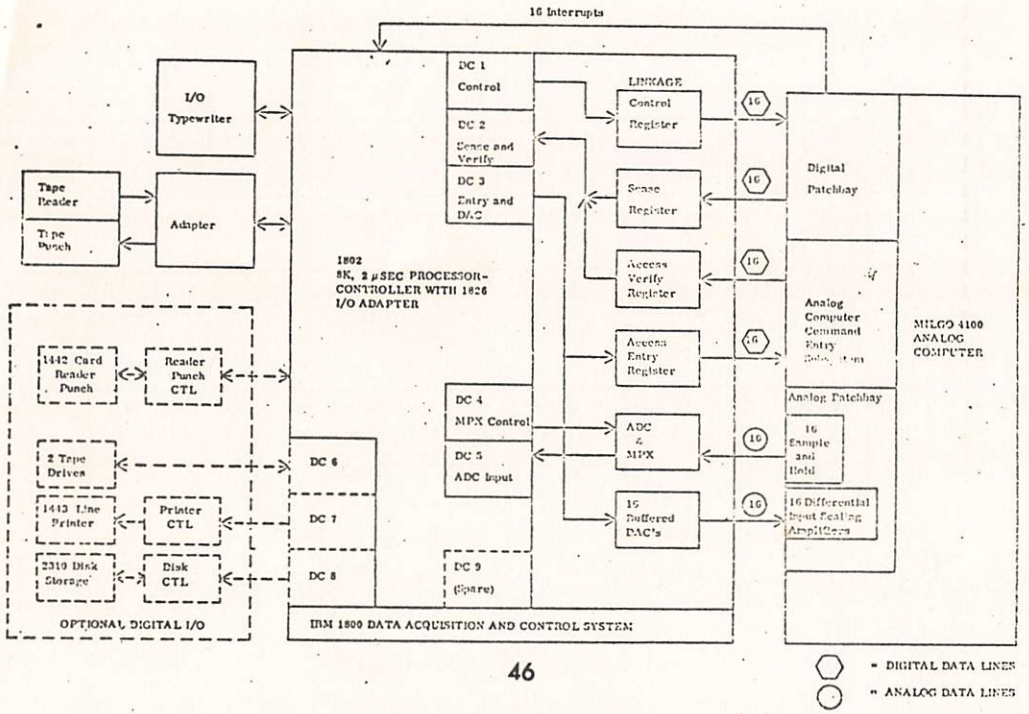

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FIGURE 2. HYBRID COMPUTING SYSTEM

APPENDIX

IBM 1800 DATA ACQUISITION AND CONTROL SYSTEM

EQUIPMENT LIST

Unit	Model or Feature #	Description	Quantity
1802	2C	Processor Controller	1
	#1232	A/D Converter	1
	#1233	Analog Input Data Channel (Adapter 1)	1
	#1234	Analog Input Data Channel (Adapter 2)	1
	#3222	Data Channel	2
	#3262	Digital Input Adapter	1
	#3285	Digital Input Contact	1
	#3286	Digital Input Voltage	2
	#3290	Digital and Analog Output Data Channel Adapter	1
	#3291	Digital Input Data Channel Adapter	1
	#3295	Digital Output Adapter	2
	#3296	Digital Output Control	2
	#5258	Multiplex "A" Control	1
	#5710	Process Interrupt Adapter	1
	#5716	Process Interrupt Voltage	1
	#6125	Register Output	2
	#7296	1054/1055 Adapter	1
1856	Mod I	Analog Output Terminal	1
	#1505	Buffer Register	16
	#3254	Digital Analog Converter Mod. 4	8
	#1227	Analog Driver Amplifier	16
1854	Mod I	Hybrid Input Terminal	1
	#4608	Hybrid Input Matching Points	2
1851	Mod I	Multiplexer Terminal	1
	#5253	Multiplexer/S	1
	#8610	Universal Element	16
	#8750	Voltage Element	16
1826	Mod II	Data Adapter Unit	1
1828	Mod II	Data Adapter Unit Enclosure Mod II	1
1816	Mod I	Printer Keyboard	1
1054	Mod I	Paper Tape Reader Mod I	1
1055	Mod I	Paper Tape Punch, Mod I	1

IBM 1800 OPTIONAL EQUIPMENT

Unit	Model or Feature #	Description	Quantity
1442	7	Card Read Punch	1
	#4430	1442 Adapter	1
1443	2	Printer	1
	#4431	1443/1627 Adapter	1
	#4432	1443 Control	1
	#5569	Printer Control for 1800	1
	#3222	Data Channel	1
2402	1	Magnetic Tape Unit	1
	#3222	Data Channel	1
	#9557	7-Track Read/Write Head	1
	#7125	7-Track Compatibility	1
2310	A1	Disk Storage	1
	#2315	Disk Cartridge	1
	#3222	Data Channel	1
	#8085	2310 Adapter	1
	#8086	2310 Disk Storage Drive Control	1